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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/747,976	12/27/2000	Takashi Kitae	56937-022	3643

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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/747,976	Applicant(s) KITAE ET AL.	
	Examiner Nitin Parekh	Art Unit 2811	

-- Th MAILING DATE of this communication appears on the cover sh t with th correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6-9 and 18-27* is/are pending in the application.

4a) Of the above claim(s) *10-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,6-9,19-21,23-25 and 27* is/are rejected.

7)☒ Claim(s) *4,18,22 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/31/03 has been entered. An action on the RCE follows.

Information Disclosure Statement

2. The Information Disclosure Statement filed on 12/27/2000 has been considered.

Oath/Declaration

3. The oath/declaration filed on 12/27/2000 is acceptable.

Drawings

4. The formal drawings filed on 12/27/2000 are acceptable.

Claim Objections

5. Claim 18 is objected to because of the following informalities:

The limitation "the particle diameter" as recited in claim 18, line 6, should read "a particle diameter".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the
>
> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 3 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sano et al. (US Pat. 5822176) in view of Seto (SETO-US Pat. 2001/0026017) and Ikeda (US Pat. 6262785).

Regarding claim 1, Sano et al. disclose an electronic part comprising:

- a chip capacitor/electronic part (1 in Fig. 1)
- an outer/external electrode (5 in Fig. 1) being formed at both ends of the part,
- a coating/plating including a layer of conductive metals/fillers such as nickel and copper being disposed on entire surface of the outer/external electrodes (6 in Fig. 1; Col. 5, line 51), and
- a conductive layer of solder being provided on the coating/plating

(Fig. 1; Col. 5, line 40- Col. 6, line 45).

Sano et al. fail to teach using :

a) the coating being a thermoplastic or thermosetting resin, and

b) the conductive layer being a conductive adhesive containing a conductive filler consisting of gold, silver, platinum, nickel, zinc, palladium, or an alloy or a mixture containing these metals.

a) Seto teaches using an external electrode (17/18/19/2 in Fig. 9) having a multilayered coating including nickel coating in a form of thermosetting resin (not numerically referenced in Fig. 9; see section-0046) being disposed on end portions of an external electrode terminal (17 in Fig. 9).

b) Ikeda teaches an electronic part having a conductive layer on external electrodes where the conductive layer comprises a conductive adhesive (Col. 3, lines 29-35; see 11 in Fig. 1 being shown only at the bottom surface of the external electrode 5) containing conductive filler consisting of metals such as silver (Ag), palladium (Pd), copper (Cu), etc (Col. 3, lines 29-35; Col. 2, line 45-57).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the coating including a thermosetting or thermoplastic resin as taught by Seto and the conductive layer being a conductive adhesive containing conductive filler consisting of gold, silver, platinum, nickel, palladium, or an alloy or a mixture containing these metals as taught by Ikeda so that

the thermal stability, conductivity and the coating layer integrity/strength can be improved in Sano et al's electronic part.

Regarding claim 3, Sano et al. teach substantially the entire claimed structure as applied to claim 1 above, including the coating containing the conductive filler consisting of gold, silver, platinum, nickel, zinc, palladium, or an alloy or a mixture containing these metals electrodes (Col. 5, line 51).

Regarding claim 27, Sano et al. teach substantially the entire claimed structure as applied to claim 1, including the coating (6 in Fig. 1) being disposed over the entire surface of the external electrode.

8. Claims 6, 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda (US Pat. 6262785) in view of Seto (SETO-US Pat. 2001/0026017).

Regarding claim 6, Ikeda discloses an electronic part mounting element (3/11 in Fig. 1) comprising:

- an electronic part (3 in Fig. 1)
- an external electrode (5 in Fig. 1) being formed at both ends of the part,

- a coating layer containing a conductive adhesive/resin ingredients being disposed on both ends/entire surface of the electrodes (not numerically referenced on the surface of 5 in Fig. 1; see lines 29-35)
- an element having a conductive adhesive layer (11 in Fig. 1) being mounted/formed on the electronic part
- a conductive adhesive layer containing conductive filler consisting of metals such as Ag, Pd, and Cu (Col. 2, line 45-57; Col. 3, lines 34-37), and
- the conductive adhesive layer electrically connecting the external electrode to connecting terminals (9 in Fig. 1; Col. 2, line 30- Col. 3, line 35) of the element to be mounted

(Fig. 1; Col. 2, line 30- Col. 3, line 35).

Ikeda fails to explicitly show the coating containing the resin ingredients in Fig. 1 being on the surface of the external electrodes.

Seto teaches using a multilayered coating including a nickel coating in a form of thermosetting resin (not numerically referenced in Fig. 9; see section-0046) being disposed on end/external portions of the electrode terminal.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the coating the containing resin ingredients being formed on the surface of the external electrodes as taught by Seto so that the thermal

stability, conductivity and the coating layer integrity/strength can be improved in Ikeda's electronic part mounting element.

Regarding claim 7, Ikeda teaches substantially the entire claimed structure as applied to claim 6 above, and further teaches the coating and the conductive adhesive being formed/combined into one element to provide an electrical and mechanical connection of the electronic part to a wiring base plate (not numerically referenced as one element in Fig. 1; see Col. 3, lines 29-37).

Regarding claim 9, Ikeda teaches substantially the entire claimed structure as applied to claim 6 above, and further teaches the coating and the conductive adhesive being formed/combined into one element (not numerically referenced as one element in Fig. 1; see Col. 3, lines 29-37) and being operative as a connecting element to provide an electrical and mechanical connection of the external electrodes of the electronic part to the connecting terminals.

9. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda (US Pat. 6262785) and Seto (SETO-US Pat. 2001/0026017) as applied to claims 6 and 7 above, and further in view of Wajima et al. (US Pat. 6274968).

Regarding claim 8, Ikeda and Seto teach substantially the entire claimed structure as applied to claims 6 and 7 above, except the joining portion of the coating with the conductive adhesive being shaped like a fillet.

Wajima et al. teach joining external/terminal electrodes (5a/2e in Fig. 3-5) having respective coating/plating with a conductive material such as conductive adhesive or solder (Col. 6, line 33) where the joining portion is shaped like a fillet (6a in Fig. 3) to improve reliability of an electrical connection (Col. 7, lines 52-58).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the joining portion of the coating with the conductive adhesive being shaped like a fillet as taught by Wajima et al. so that the reliability, adhesion and bonding strength of the external electrodes can be improved in Seto and Ikeda's electronic part mounting element.

10. Claims 19 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sano et al. (US Pat. 5822176), Seto (SETO-US Pat. 2001/0026017) and Ikeda (US Pat. 6262785) as applied to claim 1 above, and further in view of Kodama et al. (US Pat. 5277723).

Regarding claim 19, Sano et al., Seto and Ikeda teach substantially the entire claimed structure as applied to claim 1 above, except a surface roughness (Ra) of the external electrode being set in a range of 0.1-10.0 microns.

Kodama et al. teach using electronic parts comprising an internal and external wiring/conductors on inside and side surfaces where the external surface has Ra value of about 1.0 micron or preferably 2.0 microns (Fig. 7c, 5c, 3c, etc.; Col. 7, line 35- Col. 8, line 20; Col. 11, line 35- Col. 12, line 55). Kodama et al further teach achieving the optimum Ra value by controlling the parameters such as firing shrinkage ratio, temperature, pressure and pore size of a substrate material (Col. 11, line 50; Col. 8-12).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to arrive at a surface roughness (Ra) range of the external electrode surface being 0.1-10 microns as taught by Kodama et al. so that the adhesion and bonding strength of the external electrodes can be improved in Ikeda, Seto and Sano et al's electronic part.

Regarding claim 23, Sano et al., Seto and Ikeda teach substantially the entire claimed structure as applied to claim 1 above, except a surface roughness (Ra) of the external electrode being set in a range of 0.1-5.0 microns.

Kodama et al. teach using electronic parts comprising an internal and external wiring/conductors on inside and side surfaces where the external surface has Ra value of about 1.0 micron or preferably 2.0 microns (Fig. 7c, 5c, 3c, etc.; Col. 7, line 35- Col. 8, line 20; Col. 11, line 35- Col. 12, line 55). Kodama et al further teach achieving the optimum Ra value by controlling the parameters such as firing shrinkage ratio, temperature, pressure and pore size of a substrate material (Col. 11, line 50; Col. 8-12).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to arrive at a surface roughness (Ra) range of the external electrode surface being 0.1-5.0 microns as taught by Kodama et al. so that the adhesion and bonding strength of the external electrodes can be improved in Seto and Sano et al's electronic part.

11. Claims 20, 24 and 21, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda (US Pat. 6262785) and Seto (SETO-US Pat. 2001/0026017) as applied to claims 6 and 9 respectively above, and further in view of Kodama et al. (US Pat. 5277723).

Regarding claim 20, Ikeda and Seto teach substantially the entire claimed structure as applied to claim 6 above, except a surface roughness (Ra) of the external electrode being set in a range of 0.1-10.0 microns.

Kodama et al. teach using electronic parts comprising an internal and external wiring/conductors on inside and side surfaces where the external surface has Ra value of about 1.0 micron or preferably 2.0 microns (Fig. 7c, 5c, 3c, etc.; Col. 7, line 35- Col. 8, line 20; Col. 11, line 35- Col. 12, line 55). Kodama et al further teach achieving the optimum Ra value by controlling the parameters such as firing shrinkage ratio, temperature, pressure and pore size of a substrate material (Col. 11, line 50; Col. 8-12).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to arrive at a surface roughness (Ra) range of the external electrode surface being 0.1-10 microns as taught by Kodama et al. so that the adhesion and bonding strength of the external electrodes can be improved in Seto and Ikeda's electronic part mounting element.

Regarding claim 24, Ikeda and Seto teach substantially the entire claimed structure as applied to claim 6 above, except a surface roughness (Ra) of the external electrode being set in a range of 0.1-5.0 microns.

Kodama et al. teach using electronic parts comprising an internal and external wiring/conductors on inside and side surfaces where the external surface has Ra value of about 1.0 micron or preferably 2.0 microns (Fig. 7c, 5c, 3c, etc.; Col. 7, line 35- Col. 8, line 20; Col. 11, line 35- Col. 12, line 55). Kodama et al further teach achieving the optimum Ra value by controlling the parameters such as firing shrinkage ratio, temperature, pressure and pore size of a substrate material (Col. 11, line 50; Col. 8-12).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to arrive at a surface roughness (Ra) range of the external electrode surface being 0.1-5.0 microns as taught by Kodama et al. so that the adhesion and bonding strength of the external electrodes can be improved in Seto and Ikeda's electronic part mounting element.

Regarding claim 21, Ikeda and Seto teach substantially the entire claimed structure as applied to claim 9 above, except a surface roughness (Ra) of the external electrode being set in a range of 0.1-10.0 microns.

Kodama et al. teach using electronic parts comprising an internal and external wiring/conductors on inside and side surfaces where the external surface has Ra value of about 1.0 micron or preferably 2.0 microns (Fig. 7c, 5c, 3c, etc.; Col. 7, line 35- Col. 8, line 20; Col. 11, line 35- Col. 12, line 55). Kodama et al further teach achieving the optimum Ra value by controlling the parameters such as firing shrinkage ratio, temperature, pressure and pore size of a substrate material (Col. 11, line 50; Col. 8-12).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to arrive at a surface roughness (Ra) range of the external electrode surface being 0.1-10 microns as taught by Kodama et al. so that the adhesion and bonding strength of the external electrodes can be improved in Seto and Ikeda's electronic part mounting element.

Regarding claim 25, Ikeda and Seto teach substantially the entire claimed structure as applied to claim 9 above, except a surface roughness (Ra) of the external electrode being set in a range of 0.1-5.0 microns.

Kodama et al. teach using electronic parts comprising an internal and external wiring/conductors on inside and side surfaces where the external surface has Ra value of about 1.0 micron or preferably 2.0 microns (Fig. 7c, 5c, 3c, etc.; Col. 7, line 35- Col.

8, line 20; Col. 11, line 35- Col. 12, line 55). Kodama et al further teach achieving the optimum Ra value by controlling the parameters such as firing shrinkage ratio, temperature, pressure and pore size of a substrate material (Col. 11, line 50; Col. 8-12).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to arrive at a surface roughness (Ra) range of the external electrode surface being 0.1-5.0 microns as taught by Kodama et al. so that the adhesion and bonding strength of the external electrodes can be improved in Seto and Ikeda's electronic part mounting element.

Allowable Subject Matter

12. Claims 4, 18, 22 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter:

The primary reason for an allowance of claims 4, 18, 22 and 26 is the inclusion of the limitations of an electronic part having an external electrode with a coating of a thermoplastic or thermosetting resin where a conductive adhesive layer having conductive particles as filler particles is disposed on the coating such the thickness of the coating is less than the particle diameter of the conductive filler. The prior art

references Sano et al. (US Pat. 5822176), Ikeda (US Pat. 6262785), Seto (SETO-US Pat. 2001/0026017), Kodama et al. (US Pat. 5277723) and Wajima et al. (US Pat. 6274968) lack the teachings of the external electrode having the coating and the conductive adhesive having filler particles where the coating is thinner than the diameter of the filler particles.

Response to Arguments

14. Applicant's arguments with respect to claims 1, 3, 6-9, 19-21, 23-25 and 27 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722, 703-308-7724 or 703-872-9318 (Right FAX) for regular communications; 703-872-9310 (Right FAX) for After Final communications and 703-872-9310 (Right FAX) for customer service.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

NP

06-10-03

Nitin Parekh

PATENT EXAMINER

TECHNOLOGY CENTER 2800